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(Use as many sheets as necessary)

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Complete if Known	
Application Number	10/086,549
Filing Date	3/4/02
First Named Inventor	YUTAKA ARIMA
Art Unit	2121
Examiner Name	Joseph P. Hirs
Attorney Docket Number	08372.0007

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]
H		YUTAKA ARIMA, "Higher Integration of Neural Network with Learning Function," Study of Associative Memory Analog Neural Network LSI with Learning Function (January 1998).	√
H		"Chaos and Associative Memory," Computer Today (July 1999).	√
H		YUTAKA ARIMA, et al., "A Self Learning Neural Network Chip with 125 Neurons and 10K Self-Organization Synapses," 26 IEEE Journal of Solid-State Circuits 607 (April 1991).	
H		YUTAKA ARIMA, et al., "A 336-Neuron, 28K-Synapse, Self-Learning Neural Network Chip with Branch-Neuron-Unit Architecture," 26 IEEE Journal of Solid-State Circuits 1637 (November 1991).	
H		YUTAKA ARIMA, et al., "A Refreshable Analog VLSI Neural Network Chip with 400 Neurons and 40K Synapses," 27 IEEE Journal of Solid-State Circuits 1854 (December 1992).	

Examiner Signature		Date Considered	1/13/05

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